CLAIMS:

1. Apparatus (10; 20) for generating a logic signal (nporst) indicating that a supply voltage (VDDA) has reached a stable level, the apparatus (10; 20) comprising

- a first unit (POR_1, 11; 21; 31) for comparing a reference voltage (vref) with a sub-voltage (input_plus) derived from the supply voltage (VDDA) in order to issue a first logic signal (out_res) when the sub-voltage (input_plus) has reached the reference voltage (vref),
- a second unit (POR_2, 12; 22) for applying a delay in order to issue a delayed logic signal (out_delay),
- a logic unit (13; 23) for combining the first logic signal (out_res) and the delayed logic signal (out_delay) in order to provide the logic signal (nporst).

2. The apparatus (10; 20) of claim 1, wherein the first unit (POR_1, 11; 21; 31) comprises a voltage divider (11.1; 21.1; 31.1) and a comparator (11.2; 21.2; 31.2).

3. The apparatus (10; 20) of claim 2, wherein the first unit (POR_1, 31) further comprises a switch (31.6) that allows a first sub-voltage (Vtrl) to be compared with the reference voltage (vref) after a reset and a second sub-voltage (Vsel) to be compared with the reference voltage (vref) after a power down.

4. The apparatus (10; 20) of claim 3, wherein a trigger signal (nporst) is applied to the switch (31.6) in order to switch it from one state to another state.

5. The apparatus (10; 20) of claim 1, 2 or 3, wherein the reference voltage

(vref) is a bandgap voltage.

6. The apparatus (10; 20) of claim 1, 2 or 3, wherein the first unit (POR_1, 21; 31) comprises an input (31.5) for programming the level of a divider voltage (Vsel), said divider voltage (Vsel) defining the delay.

7. The apparatus (10; 20) of claim 1, wherein the second unit (POR_2, 12; 22; 32) comprises a delay unit (12.1), or a fixed delay unit (22.1) followed by a comparator (22.2).

8. The apparatus (10; 20) of claim 1, wherein the second unit (POR_2, 12) comprises an input (18) for programming the level of a divider voltage (Vsel), said divider voltage (Vsel) defining the delay.

9. The apparatus (10; 20) of one of the preceding claims, wherein the logic unit (13; 23) comprises a two-port AND gate.

10. Method for generating a logic signal (nporst) in an integrated circuit indicating that a supply voltage (VDDA) has reached a stable level comprising the steps:

- providing a reference voltage (vref),
- comparing a sub-voltage (input_plus) of the supply voltage (VDDA) with the reference voltage (vref) in order to provide a first logic output signal (out_res) when the sub-voltage (input_plus) reaches the reference voltage (vref),
- providing a second logic output signal (out_delay) that is delayed with respect to the supply voltage (VDDA),
- combining the first logic output signal (out_res) and the second logic output signal (out_delay) to switch the logic signal (nporst) from one state to another state if the first logic output signal (out_res) and the second logic output signal (out_delay) have the same logic value,
- starting an application within the integrated circuit.

11. The method of claim 10, whereby the logic signal (nporst) becomes a logic "1" if the first logic output signal (out_res) and the second logic output signal (out_delay) both represent a logic "1".

12. The method of claim 10 or 11, comprising the step of programming the delay for providing the second logic output signal (out_delay).

13. Integrated circuit comprising an apparatus according to one of the claims 1 through 9 and further comprising circuitry requiring a certain stability of the supply voltage (VDDA) before initiating operation.